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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,997	07/08/2003	Dennis Harold Burke JR.	TI34951	8166

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EXAMINER	
CHUNG, PHUNG M	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,997	BURKE ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-15 and 17-34* is/are rejected.

7)☒ Claim(s) *3 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-2, 4-15 and 17-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugamori (6,536,006).

As per claim 1, Sugamori discloses a method of testing at least one mixed signal semiconductor device:

Preparing execution of a second test for at least one mixed signal semiconductor device concurrently with the executing of the first test;

Processing test data resulting from the first test; and

Executing the second test concurrently. (See col. 9, lines 66-67 to col. 10, lines 1-7 and col. 11, lines 66-67 to col. 12, lines 1-22).

As per claim 2, Sugamori further discloses wherein the mixed signal semiconductor testing a performed by a single processor (67).

As per claim 4, further identifying hardware elements corresponding to the second test; and configuring the hardware elements corresponding to the second test is inherent in the system of Sugamori.

As per claims 5-6, Sugamori does not disclose that wherein the first and second tests are configured for one or more of wafer testing and package testing of the mixed signal semiconductor device. However, it would have been obvious to a person of ordinary skill in the electronic art, at the time the invention was made, to set the first and second tests to configure for one or more of wafer testing and package testing of the mixed signal semiconductor device. This is because Sugamori discloses semiconductor test system for testing analog/digital mixed signal integrated circuit. (See col. 7, lines 30-55).

As per claims 7-11, Sugamori does not disclose wherein the interpreted software language is interactive test pascal. However, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to interpreted software language as interactive test pascal. This is because Sugamori discloses it is possible to formulate an overall test system having different hardware and software therein. (See col. 5, lines 5-15).

As per claims 12-14, Sugamori discloses an apparatus for testing at least one mixed signal semiconductor device, the apparatus comprising:

At least one processor (67); and

At least one device tester unit (19) coupled to the processor, wherein the processor is configure to:

Execute a first test for the at least one mixed signal semiconductor device;

Prepare execution for a second test..;;

Process test data resulting from the first test; and

Execute the second test.... (See col. 9, lines 66-67 to col. 10, lines 1-7 and col. 11, lines 66-67 to col. 12, lines 1-22).

As per claim 15, this claim is rejected under similar rationale as set forth in claim 2.

As per claim 17, this claim is rejected under similar rationale as set forth in claim 4.

As per claims 18-19, these claims are rejected under similar rationale as set forth in claims 5-6.

As per claim 20, this claim is rejected under similar rationale as set forth in claim 7.

As per claims 21-34, these claims are rejected under similar rationale as set forth in claims 7-11.

3. Claims 3 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner
Art Unit 2138